Express Mail Number EV342470480US

PATENT

ESD PROTECTION CIRCUIT FOR HIGH-VOLTAGE, HIGH DV/DT PADS

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view illustrating an example of an ESD protection circuit 100 in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 shows a schematic view that illustrates an example of an electrostatic discharge (ESD) protection circuit 100 in accordance with the present invention. As described in greater detail below, circuit 100 utilizes a bipolar transistor that is connected to a pad to provide ESD protection for the pad, and a MOS transistor that is connected to the bipolar transistor to turn off the bipolar transistor during normal circuit operation.

As shown in FIG. 1, ESD protection circuit 100 includes a pad 110, and a bipolar transistor Q1 that has a collector connected to pad 110, a base, and an emitter connected to a ground line. In addition, as shown by the dashed lines, transistor Q1 also has a parasitic base-to-collector capacitance C1. (Capacitance C1 can be increased by connecting a capacitor between and to the base and collector of transistor Q1.)

ESD protection circuit 100 further includes a resistor R1 that is formed between the base and emitter of transistor Q1, a to-be-protected 112 circuit, and a MOS transistor M1. To-be-protected circuit 112 can be, for example, the gate of a MOS transistor. MOS transistor M1, in turn, has a drain that is connected to the base of transistor Q1, a gate, and a source that is connected to the ground line.

In addition, ESD protection circuit 100 includes a resistor R2 that is connected between the gate of transistor M1 and the ground line, and a delay line 114 that is connected to the gate of transistor M1. Delay line 114, which can be implemented as, for example, an RC delay of approximately one microsecond, is also connected to a power supply line VDD.

In operation, when an ESD event occurs on pad 110 with respect to the ground line, the voltage on pad 110 rises quickly which, in turn, causes the voltage on the base of transistor Q1 to also rise quickly due to the base-to-collector capacitance, thereby turning on transistor Q1. When transistor Q1 turns on, transistor Q1 provides a low impedance path from pad 110 (the pad experiencing the ESD event) to the ground line. As a result, transistor Q1 is able to absorb the large ESD current pulse while keeping the voltage on pad 110 sufficiently low enough as to not damage to-be-protected circuit 112.

In the present example, transistor Q1 is a high-voltage transistor that is formed to not breakdown when, for example, a normal operating voltage of 50V is placed on pad 110. When a lower normal operating voltage is used, such as 1.8V, transistor Q1 can be formed so that, when an ESD event occurs, the rising voltage on pad 110 breaks down the reverse-biased base-to-collector junction. The broken down junction, in turn, injects holes into the base of transistor Q1. The increased number of holes and the resulting current flow through resistor R1 causes the voltage on the base of bipolar transistor Q1 to rise quickly, thereby turning on transistor Q1.

In the event that pad 110 and the pad that provides the supply voltage VDD are the same pad and are zapped and experience an ESD event, delay line 114 provides a delay that is longer than the ESD event, which is approximately one microsecond. Thus, by the time that any

voltage due to the ESD event has propagated through delay line 114 to transistor M1, transistor Q1 has already turned on and discharged the ESD event.

Once a chip that includes ESD protection circuit 100 has been installed in a circuit board and power has been provided to the board, the supply voltage VDD turns on transistor M1 which, in turn, pulls the voltage on the base of transistor Q1 to zero. When the voltage on the base of transistor Q1 is pulled to zero, transistor Q1 is turned off.

As a result, when high-voltage signals with a very fast rising edge (high dV/dt) are received on pad 110, even signals with a rising edge that is less than one microsecond, transistor Q1 is prevented from turning on since the base of transistor Q1 has been pulled to ground. As a result, fast and noisy high-voltage signals on pad 110 are prevented from falsely triggering transistor Q1.

Circuit 100 does not protect to-be-protected circuit 112 from ESD events during normal circuit operation. ESD events, however, typically happen to chips during handling or circuit board assembly, and not while the chips are permanently fixed in a printed circuit board and operating normally.

It should be understood that the above descriptions are examples of the present invention, and that various alternatives of the invention described herein may be employed in practicing the invention. Thus, it is intended that the following claims define the scope of the invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.